Cycle-Time Improvements for Photolithography Process in Semiconductor Manufacturing

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***Abstract*—Cycle-time reduction is of great importance to semiconductor manufacturers. Photolithography, being one of the most repeated processes, is an area where substantial improvements can be made. We investigate the effects of various process control mechanisms for photolithography on the cycle-time at the process and at the overall fab via a simulation study. Test run policy at the photolithography station, test run frequency, duration of inspection, and machine dedication policy for the equipment are the factors we consider. Equipment down time due to preventive or breakdown maintenance and rework rates are also taken into account. Parallel testing, where test wafer is inspected while the lot is being processed, is the best policy in terms of cycle-time performance. Long inspection time and infrequent, long down times have the most adverse effects, but flexible machine assignment may reduce the impact of down times. Test run frequency is only significant for serial testing, where processing of the lot is not finished until the failed test wafer is stripped and reworked.**

***Index Terms*—Cycle time, dispatching, machine dedication, photolithography, shop-floor control.**

I. INTRODUCTION

IN SEMICONDUCTOR manufacturing, the *cycle-time*, also known as the turn-around time, is the length of time from bare silicon wafer start to final test. Cycle-time consists of queueing time for the equipment, waiting time due to preventive/breakdown maintenance or engineering hold, processing time, inspection time, and transportation time. Semiconductor manufacturers strive to reduce the cycle-time by simplifying the process and design and by improving the production control mechanisms for effective scheduling, better dispatching, and improved line balance. Increasing tool availability and reliability, improving the layout for effective material handling, and batch size changes to reduce queueing times or to decrease setups are some other measures that may be taken. With shorter cycle-times, a manufacturer can fill customer orders more quickly and be more responsive to the market. Furthermore, as the cycle-time gets shorter, problems in the process can be diagnosed quicker, allowing for faster process development and refinement. Consequently, the firm can improve its yield more rapidly. Thus, semiconductor manufacturers exercise strict control over the cycle-time and make continuous efforts to reduce it to remain competitive.

Photolithography is usually the bottleneck process with the most expensive equipment in a wafer fab. Being one of the processes that is repeated the most during fabrication, any reduction in photolithography cycle-time will reduce overall fab cycle-time. Leachman *et al.* [2] state that the leading fabs in the industry exhibit solid improvement trends in photolithography equipment productivity over the past decade. This suggests that photolithography is an area where substantial improvements can be made in terms of cycle-time reduction.

In this study, we examine the effects of different test run and machine dedication policies for photolithography on both the station and fab cycle-times. The following section presents a description of the photolithography process and a discussion of the policies we consider in our study. Section III describes the system under study. Section IV presents the simulation model used and the performance measures considered. Sections V and VI discuss the experimental design and the results of the experiments respectively. The final section of the paper summarizes the study, presents the conclusions, and discusses future research directions.

II. THE PHOTOLITHOGRAPHY PROCESS

During photolithography, the circuit patterns are transferred onto the wafer. The first photolithography operation is to coat the wafer with photo-resist. The wafer is then baked to firm the photo-resist and improve its adhesion to the wafer before it is sent to an aligner or a stepper for exposure. In the case of a stepper, a *reticle*, a template containing the pattern for only a few chips, is placed on the wafer and exposed to ultraviolet (UV) light. The alignment and exposure process, which constitutes a *step*, is repeated until the whole wafer surface is exposed. Each layer requires a different mask/reticle specifically designed for that layer's device characteristics. The wafer is then sent for developing, where the exposed photo-resist is removed with a special solvent, after which it goes through the final bake to ensure that the unexposed photo-resist adheres to the wafer.

The process control practices and dispatching affect the cycle-time of photolithography (PL). Several authors have studied cycle-time reduction for PL [6]–[8]. In our study, we address the same question. Now we discuss the process control decision we consider and try to develop an intuitive understanding on how these decisions and equipment properties affect the cycle-time.

PL is a critical process, since meeting tolerances on the critical dimensions (line width, spacing, and contact dimensions) and alignment with the previous layers is necessary to

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the operation of the circuit [9]. In order to check conformance to process specifications, test runs are made regularly. In a test run, a single wafer from the lot is processed and then inspected. If the test wafer meets specifications, the stepper is qualified for the process. If it fails, however, parameters of the stepper need to be adjusted and test runs are repeated until the stepper is qualified. The defective layer on the test wafer is removed by stripping the resist and the wafer is reprocessed during PL. The inspection and rework strategies have been addressed previously by Zargar [10], where both queueing models and simulation are used to study their impact on cycle-time.

Usually a test run is required every time the reticle on the stepper is changed, and after the processing of a certain number of lots. Both how the test run is made and how frequently it is made are important. Unless test wafer inspection and processing of the lot are performed simultaneously, a test run is longer than a regular production run. If the test wafer is conforming, the cycle-time of the lot is increased only by the duration of the inspection. However, if the test wafer is nonconforming, the cycle-time of the test lot is increased by the several inspections conducted and the time it takes to rework the nonconforming test wafer(s). If the inspection time is long, the increase in the lead time will be more substantial. The test run frequency also has an adverse effect on cycle-time. Increasing the number of test runs means an increased number of disruptions to ongoing processing, resulting in an increase in the average cycle-time for lots.

Processing all the layers of a lot on the same stepper assures better alignment of separate layers. Therefore, it is a common practice in industry to *dedicate* lots to PL equipment, i.e., to process all the layers of a given lot by the same stepper. If lots are dedicated to steppers, even though there may be some idle steppers, a lot waits until its stepper becomes available. Hence, the cycle-time under the dedicated policy is expected to be longer than under the flexible policy, where a lot can be processed on any available stepper.

When a test wafer fails to pass either the critical dimension measurement or the alignment test, the equipment is disqualified for processing and must be adjusted. The stepper disqualification rate is defined as the probability that the test wafers fail to pass the inspections. This rate is a function of the reliability of the lens or optics as well as how often the reticle on it is changed. If the reticle is changed too frequently, test wafer failures are more likely. Higher disqualification has an adverse affect on cycle-time, since more test wafers fail and the cycle-time for many test lots increase.

The criticality of the process coupled with the high cost of the PL equipment forces manufacturers to make frequent condition checks on the equipment. A condition check or an unpredicted breakdown take the equipment offline and a test run is required when it comes online again. As the PL equipment is highly utilized, the number of times and the duration that they are offline may affect the cycle-time adversely.

Over the past 15 years, the wafer diameter has increased to benefit from economies of scale. However, the increase in wafer diameter causes more variation in the uniformity of the resist film thickness adversely affecting the performance of the photolithography process. Advances in process technology have also been decreasing device sizes, resulting in tighter tolerances that require more frequent test runs for process control. The increase in wafer diameter also increases the inspection times. Under these circumstances, semiconductor manufacturers want to know what policies best mitigate the adverse affects of these trends on cycle-time performance. In our study, we study how test run frequency, inspection time, equipment disqualification rate, and equipment availability affect the cycle-time under a given combination of the test run and machine dedication policies. By doing so, we hope to explore the effects of process control decisions and other process factors on cycle-time.

III. SYSTEM DESCRIPTION

In this study, a manufacturing line producing a single dynamic random access memory (DRAM) product requiring more than 300 operations with 21 mask layers is considered. The model developed is a scaled down representation of this line with 36 operations for nine layers. The process flow is given in Table I. Some photolithography layers are more critical to the operation of the device than the others and the process is more strictly controlled for these layers. In our model, six out of nine layer are critical and are referred to as fine layers. The test run policies, machine dedication policies, and the dispatch rules are in effect for these fine layers only.

A. Test Run Policies

We consider three different test run policies:

1) Policy 1 (P1)—Test Wafer Joins its Lot after Rework: When a test run has to be made, a single wafer from the lot is processed and inspected. If the test wafer passes inspection, the stepper is qualified to process. Upon the completion of the rest of the lot, the test wafer joins the lot. If the test wafer fails the inspection, however, the defective test wafer is stripped, while the parameters of the stepper are adjusted and another test run is made. This procedure may be repeated several times until the stepper is qualified for the process. After the successful test run, the stepper processes the rest of the lot and waits to rework the test wafer. After the stripped defective test wafer is reworked, it is matched with the rest of its lot and directed into the fab for further processing.

2) Policy 2 (P2)—Test Wafers Form a New Lot for Rework: This policy differs from the previous one only in the treatment of defective test wafers. If the test wafer fails inspection, it is stripped while the stepper is being adjusted and qualified for the process. After the successful test run and the completion of the processing of the remaining wafers in the lot, it is directed into the fab without waiting for the rework of the defective test wafer. The reworked test wafers from 6 different fine layers are stored in separate cassettes in the stripping area. Once 25 stripped test wafers are collected, this new lot is redirected to photolithography for rework.

3) Policy 3 (P3)—Test Wafer is Reworked with its Lot: When a test run has to be made, all wafers in the lot are started for processing, and the first wafer to come out of the stepper is inspected. If this wafer fails the inspection, processing is not interrupted and the entire lot is sent to stripping, while the stepper is adjusted and another test run is made. This procedure may

TABLE I
SIMPLIFIED PROCESS FLOW FOR NINE-LAYER DRAM PRODUCT

Layer	Operation
1	Rough Photolithography
	Etching 1
	Resist Stripping
	Diffusion 1
2	Fine Photolithography
	Etching 1
	Resist Stripping
	Diffusion 2
3	Rough Photolithography
	Medium Current Ion Implantation
	Resist Stripping
	Annealing
4	Fine Photolithography
	Etching 2
	Resist Stripping
	Oxidation
5	Rough Photolithography
	High Current Ion Implantation
	Resist Stripping
	Chemical Vapor Deposition
6	Fine Photolithography
	Etching 3
	Resist Stripping
	Chemical Vapor Deposition
7	Fine Photolithography
	Etching 4
	Resist Stripping
	Chemical Vapor Deposition
8	Fine Photolithography
	Etching 3
	Resist Stripping
	Metalization
9	Fine Photolithography
	Etching 4
	Resist Stripping
	Metalization

be repeated several times until the stepper is qualified for processing. The defective lot is reworked after stripping.

With P1 and P3, all the wafers of a lot move together during the entire fabrication process. With these policies, if a defect is detected at probe test, it can be attributed to the entire lot. With P2, however, wafers from different lots are combined into new lots after stripping. When a defect is detected at probe test, tracing the lot that has the defect might prove to be a difficult task, unless the inventory is tracked wafer by wafer.

B. Machine Dedication Policies

In the system under consideration, there are two different prevailing policies. Under the *dedicated assignment policy,* a lot is processed by the same stepper at all layers. In our model, we have 5 steppers allocated to the critical layers, so every sixth lot is assigned to the same stepper. The decision as to which stepper the lot is originally assigned to is cyclic aiming to balance the workload of steppers. On the other hand, under the *flexible assignment policy,* a lot can be processed by any of the steppers at any layer.

C. Dispatch Rules

A previous study by McGuigan [4] studies simple lot prioritization procedures for PL. In our study we consider more sophisticated dispatch rules for both flexible and dedicated stepper assignment policies.

Under the flexible assignment policy, every time a lot enters the station, the system is checked. If all steppers are busy, the lot is placed in the main buffer. If there are any idle steppers, we check whether any of them has the required reticle on it. If there is an idle stepper with the required reticle on it, the lot is assigned to that stepper. If there is no idle stepper with the required reticle on it, then the lot is assigned to one of the idle steppers and the reticle is changed. Note that this is a very aggressive dispatch rule, because even if there is a busy stepper with the required reticle, the lot does not wait until that stepper is idle but immediately is assigned to a stepper. When a stepper becomes idle, the system status is checked again. If there is a lot in the buffer (at any rank in the buffer) that requires the reticle on the stepper, that lot is assigned to the stepper. If there is no such lot in the buffer, the first ranked lot in the buffer is assigned to the stepper and a reticle change is scheduled. If there are no lots in the buffer, the stepper remains idle.

The dispatch rule under the dedicated assignment policy differs slightly from that under flexible assignment. When a lot enters the station, only the status of the stepper to which it has been assigned is checked. If this stepper is busy, the lot is placed in the main buffer. If the stepper is idle, the lot is assigned to it. If the stepper does not have the required reticle on it, a reticle change is also scheduled. When a stepper becomes idle, the stepper buffer is checked. Among all the lots that are waiting for the stepper, the lot that requires the reticle on the stepper is assigned to the stepper. If there is no such lot, the first lot in the buffer is assigned to the stepper and a reticle change is scheduled. If there is no lot waiting for the stepper, the stepper remains idle.

These dispatching rules process lots in first-in–first-out (FIFO) order. In many wafer fabs, due date related rules such as Critical Ratio are used. However, our main focus here is to examine the effect of dedication and test wafer policies on the cycle-time performance of the fab. Hence, we use FIFO to simplify the experimentation, as it eliminates the need for parameterization and estimates of cycle times from a given photo operation to the end of the process, as well as the issue of how due dates are set. A due date-based rule could easily be implemented in our framework and is unlikely to substantially alter the cycle time results we focus on.

IV. SIMULATION MODEL

The simulation model has been developed using SIMAN [5] supported by a Unix C Language insert. The fab is represented by a network of stations where each process step (PL, ion implantation, etching, film growth, resist stripping, etc.) is modeled as a separate station. The PL process, being the main focus

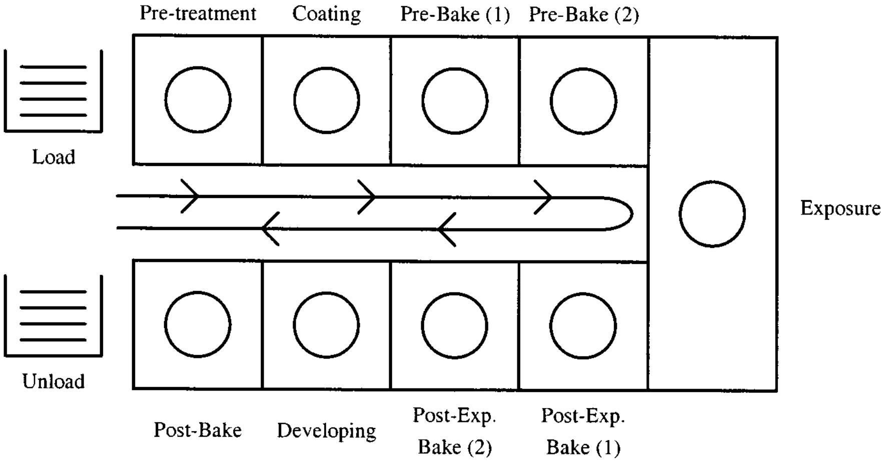

Fig. 1. Pictorial representation of a cluster stepper.

of this study, is modeled in detail while the other processes are modeled at a more abstract level. We assume all processes in the fab follow a FIFO dispatch rule except for PL. Transportation times between stations and operators are not modeled. The input rate is constant at 500 wafer starts per day with a deterministic interarrival time of 72 min.

We assume that any layer can be processed on any stepper and model the PL station as parallel identical clustered steppers. A clustered stepper, as illustrated in Fig. 1, consists of two load locks, where the wafers enter and exit the cluster, and nine process modules perform pretreatment, coating, preexposure bake, exposure, postexposure bake, developing, and postbake operations sequentially. Transfer modules transport the wafers between the process modules. A clustered stepper processes a lot in 66 min and the reticle change on the exposure tool takes from 0.5 to 1 min.

Some of the steppers, *fine layer* steppers, are dedicated to the processing of the critical layers. The remaining ones, *rough layer* steppers, are dedicated to the processing of the noncritical layers. There are separate buffers of infinite size for critical and noncritical layers. There is a single inspection station for each of the critical dimensions and the alignment measurements are in series with the fine layer steppers. The preventive maintenance schedules includes periodic condition checks (down for 6 h once a month) and lamp changes (down for 1 h once a week). We also consider unscheduled breakdowns, for which we test two scenarios: frequent breakdowns with short repair times versus rare breakdowns with long repair times limiting the total duration of unscheduled breakdowns to 2% of the total available time based on our industrial experience. The distributions for time to fail and time to repair are assumed to be exponential and gamma, respectively.

The etching, ion-implantation, metallization, low-pressure chemical vapor deposition, oxidation, diffusion, annealing, and resist stripping processes are modeled as stations with parallel identical servers. Each station has a buffer of infinite size. The number of servers at each workstation, processing times, and batch sizes are summarized in Table II.

For model validation, we used the concept of the X *factor*. Raw processing time (RPT) is the time it would take to process one lot assuming no tool breakdowns, no queueing, no rework, and no waiting. Usually, the cycle-time in a fab should be from $3\times$ to $6\times$, i.e., *three or six times RPT* [3]. In our model, where the operators, precleaning operations, and transportation are not modeled, we expect to be on the low side of this range. After test runs with the base case setting, we obtained an average cycle-time that is approximately $4\times$ RPT and the stepper utilization at around 84%. PL remains the true bottleneck of the system, as we verify the utilization levels to be below 85% at all nonbottleneck processes.

Our primary performance measures are the average and coefficient of variation of PL cycle-time and overall fab cycle-time. We also consider the number of test runs required as a surrogate measure of how much production could be disrupted and how many rework wafers/lots could be seen in the system.

V. EXPERIMENTATION

We designed our experiments to determine the effects of process control policies at PL on the average and the coefficient of variation of the cycle-time of the overall fab as well as the cycle-time at PL. Three test run policies with two machine dedication policies subject to two levels of inspection time (A), two levels of stepper disqualification rate (B), two breakdown scenarios (C), and two levels of test run frequency (D) are tested. The levels of the factors are given in Table III. Six system settings using two machine dedication and three test run policies are established, and, for each setting, 16 (2*2*2*2) scenarios are developed.

The simulation experiments are conducted under steady-state conditions. The system is started empty and idle and a single run is made to collect 32 batches of data. A batch is defined as 3600 lots (corresponding to 6 months' output). The first two batches of 7200 observations, i.e., output of a year approximately, are discarded to eliminate the initial bias. The duration of the initial transient is determined by visual inspection of data series.

Common random numbers are used for the breakdowns of the steppers for variance reduction [1]. The mean and the precision of the estimate for the performance measures are calculated using the method of batch means [1].

TABLE II
PROCESS INFORMATION FOR ALL STATIONS

Process	Station	Number of Servers	Processing Time (min.)	Batch Size (wafers)
Photolithography	Fine	6	66	25
	Rough	3	66	25
Etching	Etching 1	3	60	25
	Etching 2	3	60	25
	Etching 3	3	60	25
	Etching 4	2	60	25
Ion Implantation	Ion Implantation Medium Current	1	10	25
	Ion Implantation High Current	2	60	25
Chemical Vapor Deposition	CVD 1	1	180	100
	CVD 2	1	120 or 150	100
Annealing	Annealing	1	60	100
Oxidation	Oxidation	1	90	100
Diffusion	Diffusion 1	1	550	100
	Diffusion 2	1	240	100
Metalization	Sputtering	3	70	25
Resist Stripping	Pre-Metal Dry Resist Stripping	3	70	50
	Post-Metal Dry Resist Stripping	1	70	50
	Pre-Metal Wet Resist Stripping	3	70	50
	Post-Metal Wet Resist Stripping	1	70	50

TABLE III
EXPERIMENTAL CONDITIONS FOR THE FACTORS

Factor	Levels
Test Run Policy	Policy 1
	Policy 2
	Policy 3
Machine Dedication Policy	Dedicated
	Flexible
Inspection Time (A)	10 minutes/wafer
	20 minutes/wafer
Stepper disqualification rate (B)	0.5 percent
	2.0 percent
Breakdowns (C)	MTTF (43,200) MTTR (864)
	MTTF (10,800) MTTR (216)
Test Run Frequency (D)	Every 4 lots
	Every 8 lots

VI. RESULTS

We analyze our results in two stages. First, we look at the estimates of the aforementioned performance measures for the six system settings subject to two breakdown scenarios. A system setting is dictated by a combination of the test run and the machine dedication policies. The factors of inspection time, stepper disqualification rate, and test run frequency are kept constant at their lower experimentation levels of 10 min/wafer, 0.5%, and every 4 lots, respectively. Second, for each of these six settings, we analyze the contribution of the remaining factors to the variability of cycle-time. The reason for our choice of analysis method lies in the distinction between controllable and uncontrollable factors of the process. The fab managers have to make decisions regarding the test run policy, machine dedication policy, and the frequency of test runs. Therefore, we refer to these as the controllable factors. The other factors of stepper disqualification rate, inspection time, and the nature of breakdowns are uncontrollable factors inherent to the process technology. However, managers must know how much they affect the cycle-time performance to guide their decisions regarding new stepper or inspection equipment purchase or management of maintenance activities to remedy the adverse effects. We also include the frequency of test runs in ANOVA analysis to observe if any interaction exists between this and other uncontrollable factors.

A. Performance Measure Estimates

Table IV tabulates the estimates for the average and the coefficient of variation of the cycle-time as well as the number of test runs. The cycle-times are longest when P1 is in effect. As the steppers remain blocked in order to rework the failed test wafer, the cycle-times are high. With P2, however, when the stepper does not have to wait to rework the failed test wafer, both the mean and the variability of the cycle-time reduce significantly. Under P3, when parallel testing is in effect, however, both the mean and the coefficient of variation of the cycle-time at PL and the overall fab cycle-time are at their lowest levels.

The flexible machine assignment policy significantly reduces both the average and the variability of the cycle-time. As any available stepper can process any lot, the waiting time at the station that accounts for a considerable portion of the cycle-time is reduced. In addition, the flexible policy reduces the adverse effect of breakdowns, as the online steppers back up any offline stepper. However, the dedicated machine assignment is favored for its potential to improve quality by eliminating variability arising from different steppers. Therefore, the estimated reduction in cycle-time has to outweigh any losses due to poorer quality in order for the flexible assignment policy to be adopted. These quality issues are beyond the scope of this study.

The number of test runs required under different scenarios is also an important measure. The number of rework wafers/lots is a ratio of the number of required test runs (i.e., the more the number of test runs, the higher the number of the rework

TABLE IV
SUMMARIZED SIMULATION RESULTS

Breakdown Scenario	Test Run Frequency	System Setting	Average Cycle Time (minutes) Mean (St. Dev)	Coef. Of Var. of Cycle Time Mean (St. Dev)	Average Time at Photo (minutes) Mean (St. Dev)	Coef. Of Var. of Time at Photo Mean (St. Dev)	Average Number of Test Runs (runs/quarter) Mean (St. Dev)
Short Frequent Breakdowns	Every 4 lots	DEDICATED-1	8,178 (54)	0.106 (0.002)	569 (0)	0.538 (0.100)	8,248 (53)
		DEDICATED-2	6,179 (40)	0.089 (0.001)	273 (0)	0.613 (0.115)	16,105 (119)
		DEDICATED-3	5,485 (35)	0.088 (0.001)	154 (0)	0.844 (0.159)	17,616 (119)
		FLEXIBLE-1	6,783 (44)	0.077 (0.001)	348 (0)	0.511 (0.096)	8,815 (58)
		FLEXIBLE-2	5,745 (44)	0.062 (0.001)	199 (0)	0.431 (0.081)	18,142 (121)
		FLEXIBLE-3	5,297 (35)	0.063 (0.001)	112 (0)	0.514 (0.097)	19,978 (129)
	Every 8 lots	DEDICATED-1	7,601 (49)	0.119 (0.002)	497 (0)	0.612 (0.114)	8,164 (57)
		DEDICATED-2	6,234 (41)	0.105 (0.001)	282 (0)	0.737 (0.138)	15,898 (125)
		DEDICATED-3	5,561 (36)	0.104 (0.001)	165 (0)	1.082 (0.204)	17366 (116)
		FLEXIBLE-1	6,514 (42)	0.074 (0.001)	311 (0)	0.505 (0.094)	8,763 (62)
		FLEXIBLE-2	5,746 (44)	0.065 (0.001)	201 (0)	0.492 (0.092)	18,073 (122)
		FLEXIBLE-3	5,279 (34)	0.054 (0.001)	111 (0)	0.556 (0.105)	20,143 (129)
Long Seldom Breakdowns	Every 4 lots	DEDICATED-1	8,437 (59)	0.157 (0.003)	609 (0)	0.632 (0.116)	8,255 (56)
		DEDICATED-2	6,252 (42)	0.110 (0.001)	284 (0)	0.741 (0.139)	15,912 (118)
		DEDICATED-3	5,540 (36)	0.103 (0.001)	163 (0)	1.077 (0.203)	17,513 (122)
		FLEXIBLE-1	6,824 (47)	0.080 (0.001)	349 (0)	0.525 (0.098)	8,828 (63)
		FLEXIBLE-2	5,759 (46)	0.068 (0.001)	202 (0)	0.516 (0.097)	18,046 (122)
		FLEXIBLE-3	5,321 (35)	0.061 (0.001)	113 (0)	0.580 (0.109)	20,053 (130)
	Every 8 lots	DEDICATED-1	7,505 (47)	0.093 (0.001)	485 (0)	0.533 (0.099)	8,188 (54)
		DEDICATED-2	6,180 (41)	0.090 (0.001)	274 (0)	0.613 (0.115)	16,151 (125)
		DEDICATED-3	5,493 (35)	0.086 (0.001)	156 (0)	0.858 (0.162)	17493 (117)
		FLEXIBLE-1	6,453 (41)	0.066 (0.001)	307 (0)	0.470 (0.088)	8,780 (59)
		FLEXIBLE-2	5,751 (44)	0.066 (0.001)	200 (0)	0.458 (0.086)	18,008 (120)
		FLEXIBLE-3	5,326 (35)	0.062 (0.001)	113 (0)	0.546 (0.103)	19,884 (129)

TABLE V
ANOVA TABLES FOR THE MEAN CYCLE-TIME

TEST RUN 1 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	315594304	315594304	1688.74	0.01
B	1	611172.1	611172.1	3.27	
C	1	1229603.9	1229603.9	6.58	0.1
D	1	285715648	285715648	1528.86	0.01
AXB	1	381371.9	381371.9	2.04	
AXC	1	551708.1	551708.1	2.95	
AXD	1	235526464	235526464	1260.30	0.01
BXC	1	31640	31639.6	0.17	
BXD	1	438976	438976	2.35	
CXD	1	731520	731520	3.91	
Error	5	934408.5	186881.7		
Total	15	841746816			

TEST RUN 2 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	83362	83362.1	2420.28	0.01
B	1	1921	1920.6	55.76	0.01
C	1	16288	16288.1	472.90	0.01
D	1	175	174.9	5.08	0.1
AXB	1	28	28.4	0.82	
AXC	1	9	8.9	0.26	
AXD	1	15	15.4	0.45	
BXC	1	24	24.3	0.70	
BXD	1	21	20.5	0.59	
CXD	1	88	87.9	2.55	
Error	5	172	34.4		
Total	15	102103			

TEST RUN 3 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	1614	1614	5.34	0.1
B	1	8	8.3	0.03	
C	1	13127	13127.4	43.43	0.01
D	1	197	196.7	0.65	
AXB	1	124	123.8	0.41	
AXC	1	634	633.8	2.10	
AXD	1	136	136.3	0.45	
BXC	1	409	409	1.35	
BXD	1	896	895.5	2.96	
CXD	1	179	178.9	0.59	
Error	5	1511	302.2		
Total	15	18835			

TEST RUN 1 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	60728900	60728900	7034.96	0.01
B	1	10105	10105.3	1.17	
C	1	4	3.7	0.00	
D	1	40957760	40957760	4744.63	0.01
AXB	1	207	206.7	0.02	
AXC	1	12992	12992.3	1.51	
AXD	1	32914608	32914608	3812.89	0.01
BXC	1	5644	5643.8	0.65	
BXD	1	1804	1804	0.21	
CXD	1	13672	13672	1.58	
Error	5	43162	8632.4		
Total	15	134688848			

TEST RUN 2 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	174306	174306.2	5170.90	0.01
B	1	3685	3684.5	109.30	0.01
C	1	462	462.2	13.71	0.025
D	1	79	79.2	2.35	
AXB	1	97	97	2.88	
AXC	1	21	20.7	0.61	
AXD	1	6	5.5	0.16	
BXC	1	2	2.1	0.06	
BXD	1	27	26.5	0.79	
CXD	1	11	10.6	0.31	
Error	5	169	33.7		
Total	15	178863			

TEST RUN 3 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	1754	1753.5	6.61	0.05
B	1	537	537.1	2.02	
C	1	141	141	0.53	
D	1	108	107.6	0.41	
AXB	1	236	236.4	0.89	
AXC	1	23	23.3	0.09	
AXD	1	6	6.4	0.02	
BXC	1	162	161.9	0.61	
BXD	1	2	2	0.01	
CXD	1	963	962.6	3.63	
Error	5	1327	265.4		
Total	15	5259			

wafers/lots) specified by the stepper disqualification rate. P1 requires the least number of test runs. When test run policy 2 or 3 is in effect, however, the number of test runs increases significantly. Under P1, while the stepper is blocked for the failed test wafer to come back from stripping to be reworked, other lots that require the same reticle accumulate in the buffer. Once the stepper reworks the stripped wafer, it can immediately process 3 (or 7) more lots depending on the required frequency of test runs. On the other hand, under P2, the duration of a test run is longer only by the inspection time than that of a regular production run, and, under P3, it is the same as a regular production run. Since lots are aggressively dispatched to idle steppers, not many lots that require the same reticle accumulate in the buffer. This approach increases the number of test runs. Finally, under P3, the photolithography cycle-time is so short that the increase in cycle-time due to increased WIP by rework lots is offset. The number of test runs is also higher under the flexible assignment policy, which is to be expected since flexible assignment policy allows for more frequent reticle changes thereby increasing the number of test runs.

Infrequent breakdowns with long repair times increase both the fab and photolithography cycle-time slightly relative to frequent breakdowns with short repair times. Also, an increase in coefficient of variation is observed. These observations support the claim that the system performance suffers more from longer breakdowns even though they might be rare. The increase is

TABLE VI
ANOVA TABLES FOR THE COEFFICIENT OF VARIATION OF THE CYCLE-TIME

TEST RUN 1 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0078	0.0078	61.25	0.01
B	1	0.0004	0.0004	2.73	
C	1	0.0066	0.0066	51.42	0.01
D	1	0.0137	0.0137	107.09	0.01
AXB	1	0.0003	0.0003	2.41	
AXC	1	0.0000	0.0000	0.13	
AXD	1	0.0045	0.0045	35.03	0.01
BXC	1	0.0001	0.0001	0.84	
BXD	1	0.0003	0.0003	2.14	
CXD	1	0.0006	0.0006	4.54	0.1
Error	5	0.0006	0.0001		
Total	15	0.0348			

TEST RUN 2 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0000	0.0000	16.42	0.01
B	1	0.0000	0.0000	2.33	
C	1	0.0011	0.0011	881.77	0.01
D	1	0.0000	0.0000	3.88	
AXB	1	0.0000	0.0000	0.11	
AXC	1	0.0000	0.0000	0.04	
AXD	1	0.0000	0.0000	2.76	
BXC	1	0.0000	0.0000	0.75	
BXD	1	0.0000	0.0000	0.00	
CXD	1	0.0000	0.0000	5.41	0.1
Error	5	0.0000	0.0000		
Total	15	0.0011			

TEST RUN 3 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0000	0.0000	0.88	
B	1	0.0000	0.0000	0.99	
C	1	0.0010	0.0010	52.91	0.01
D	1	0.0001	0.0001	2.70	
AXB	1	0.0000	0.0000	2.08	
AXC	1	0.0000	0.0000	1.98	
AXD	1	0.0000	0.0000	0.46	
BXC	1	0.0000	0.0000	0.30	
BXD	1	0.0000	0.0000	0.95	
CXD	1	0.0001	0.0001	2.55	
Error	5	0.0001	0.0000		
Total	15	0.0013			

TEST RUN 1 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0005	0.0005	31.02	0.01
B	1	0.0001	0.0001	8.39	0.05
C	1	0.0002	0.0002	9.57	0.05
D	1	0.0009	0.0009	54.30	0.01
AXB	1	0.0001	0.0001	7.55	0.05
AXC	1	0.0000	0.0000	0.05	
AXD	1	0.0002	0.0002	10.74	0.025
BXC	1	0.0000	0.0000	0.22	
BXD	1	0.0001	0.0001	3.84	
CXD	1	0.0000	0.0000	0.09	
Error	5	0.0001	0.0000		
Total	15	0.0021			

TEST RUN 2 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0000	0.0000	5.63	0.1
B	1	0.0000	0.0000	3.12	
C	1	0.0000	0.0000	11.45	0.025
D	1	0.0000	0.0000	0.18	
AXB	1	0.0000	0.0000	0.01	
AXC	1	0.0000	0.0000	0.10	
AXD	1	0.0000	0.0000	0.05	
BXC	1	0.0000	0.0000	0.01	
BXD	1	0.0000	0.0000	4.01	
CXD	1	0.0000	0.0000	2.78	
Error	5	0.0000	0.0000		
Total	15	0.0001			

TEST RUN 3 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0000	0.0000	0.02	
B	1	0.0000	0.0000	0.60	
C	1	0.0001	0.0001	2.51	
D	1	0.0000	0.0000	0.40	
AXB	1	0.0000	0.0000	0.07	
AXC	1	0.0000	0.0000	0.90	
AXD	1	0.0000	0.0000	0.88	
BXC	1	0.0001	0.0001	2.86	
BXD	1	0.0000	0.0000	0.07	
CXD	1	0.0000	0.0000	0.60	
Error	5	0.0001	0.0000		
Total	15	0.0003			

TABLE VII
ANOVA TABLES FOR THE MEAN CYCLE-TIME AT PHOTOLITHOGRAPHY

TEST RUN 1 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	8091039.5	8091039.5	1590.38	0.01
B	1	16673.3	16673.3	3.28	
C	1	31764.2	31764.2	6.24	0.1
D	1	7133306	7133306	1402.13	0.01
AXB	1	10254.2	10254.2	2.02	
AXC	1	15466.8	15466.8	3.04	
AXD	1	6079556	6079556	1195.00	0.01
BXC	1	782.6	782.6	0.15	
BXD	1	12172	12172	2.39	
CXD	1	20370	20370	4.00	
Error	5	25437.4	5087.5		
Total	15	21436822			

TEST RUN 2 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	2495	2495	9078.81	0.01
B	1	2.7	2.7	9.91	0.05
C	1	346	346	1258.88	0.01
D	1	1.8	1.8	6.63	0.05
AXB	1	0.4	0.4	1.31	
AXC	1	0.1	0.1	0.23	
AXD	1	0	0	0.00	
BXC	1	0.1	0.1	0.23	
BXD	1	0	0	0.04	
CXD	1	1.8	1.8	6.63	0.05
Error	5	1.4	0.3		
Total	15	2849.2			

TEST RUN 3 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	52.9	52.9	6.74	0.05
B	1	0.5	0.5	0.07	
C	1	316	316	40.25	0.01
D	1	3.9	3.9	0.50	
AXB	1	8.6	8.6	1.09	
AXC	1	14.3	14.3	1.82	
AXD	1	5.9	5.9	0.75	
BXC	1	2.3	2.3	0.30	
BXD	1	13.5	13.5	1.72	
CXD	1	5.4	5.4	0.69	
Error	5	39.3	7.9		
Total	15	462.5			

TEST RUN 1 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	864342.1	864342.1	6156.81	0.01
B	1	198.8	198.8	1.42	
C	1	66.4	66.4	0.47	
D	1	586909.1	586909.1	4180.62	0.01
AXB	1	3.8	3.8	0.03	
AXC	1	219	219	1.56	
AXD	1	469156.9	469156.9	3341.86	0.01
BXC	1	82.8	82.8	0.59	
BXD	1	52.6	52.6	0.37	
CXD	1	225.1	225.1	1.60	
Error	5	701.9	140.4		
Total	15	1921958.4			

TEST RUN 2 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	5354.6	5354.6	6264.21	0.01
B	1	2.3	2.3	2.72	
C	1	6.9	6.9	8.06	0.05
D	1	1.3	1.3	1.48	
AXB	1	0.5	0.5	0.61	
AXC	1	0.6	0.6	0.70	
AXD	1	0.1	0.1	0.06	
BXC	1	0.3	0.3	0.32	
BXD	1	3.2	3.2	3.69	
CXD	1	0.1	0.1	0.16	
Error	5	4.3	0.9		
Total	15	5374.1			

TEST RUN 3 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	111.8	111.8	147.22	0.01
B	1	8.3	8.3	10.88	0.025
C	1	1.4	1.4	1.82	
D	1	1.9	1.9	2.49	
AXB	1	0.1	0.1	0.07	
AXC	1	0.5	0.5	0.69	
AXD	1	0.4	0.4	0.51	
BXC	1	1.5	1.5	1.98	
BXD	1	0	0	0.04	
CXD	1	2.3	2.3	3.06	
Error	5	3.8	0.8		
Total	15	132			

more significant under dedicated machine assignment. Breakdowns do not significantly effect on the number of required test runs.

The frequency of test runs has the most significant adverse effect under P1. As the number of test runs increase, so does the amount of time the stepper remains blocked. As a result, the lead time at PL and overall cycle-times are increased more significantly. However, it does not seem to have such a significant effect under the other test run policies.

B. Analysis of Variance (ANOVA)

Results of an analysis of variance (ANOVA) study for the average cycle-time are tabulated in Table V. For all test run and machine dedication policies, the inspection time seems to be the factor with most significant effect. As P2 requires very frequent test runs, the adverse impact of stepper disqualification rate on the cycle-time becomes significant for this policy. The frequency of test runs and its interaction with inspection time are significant only for P1. As the steppers are blocked for rework test wafers, the increase in test run frequency, which causes more lots to spend more time at PL, significantly affects the cycle-time. An interesting observation from this table is that the change in machine dedication policy from dedicated to flexible reduces the adverse effect of breakdowns on the cycle-time. As other steppers can back up the offline stepper, the processing rate at the station, consequently the cycle-time, is not signif-

TABLE VIII
ANOVA TABLES FOR THE COEFFICIENT OF VARIATION OF THE CYCLE-TIME AT PHOTOLITHOGRAPHY

TEST RUN 1 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Sig
A	1	0.0202	0.0202	162.47	0.01
B	1	0.0000	0.0000	0.03	
C	1	0.0161	0.0161	129.46	0.01
D	1	0.0027	0.0027	21.73	0.01
AXB	1	0.0001	0.0001	1.03	
AXC	1	0.0018	0.0018	14.44	0.025
AXD	1	0.0058	0.0058	46.75	0.01
BXC	1	0.0001	0.0001	0.50	
BXD	1	0.0000	0.0000	0.21	
CXD	1	0.0002	0.0002	1.25	
Error	5	0.0006	0.0001		
Total	15	0.0476			

TEST RUN 2 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0062	0.0062	369.60	0.01
B	1	0.0000	0.0000	0.54	
C	1	0.0628	0.0628	3738.01	0.01
D	1	0.0000	0.0000	0.95	
AXB	1	0.0000	0.0000	2.25	
AXC	1	0.0001	0.0001	7.40	0.05
AXD	1	0.0000	0.0000	0.00	
BXC	1	0.0000	0.0000	0.55	
BXD	1	0.0000	0.0000	0.08	
CXD	1	0.0000	0.0000	1.29	
Error	5	0.0001	0.0000		
Total	15	0.0693			

TEST RUN 3 - DEDICATED ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0084	0.0084	2.02	
B	1	0.0038	0.0038	0.92	
C	1	0.1684	0.1684	40.29	0.01
D	1	0.0023	0.0023	0.55	
AXB	1	0.0044	0.0044	1.04	
AXC	1	0.0037	0.0037	0.88	
AXD	1	0.0044	0.0044	1.05	
BXC	1	0.0020	0.0020	0.48	
BXD	1	0.0049	0.0049	1.16	
CXD	1	0.0020	0.0020	0.48	
Error	5	0.0209	0.0042		
Total	15	0.2252			

TEST RUN 1 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0015	0.0015	56.85	0.01
B	1	0.0000	0.0000	1.75	
C	1	0.0018	0.0018	68.24	0.01
D	1	0.0019	0.0019	71.29	0.01
AXB	1	0.0003	0.0003	9.25	0.05
AXC	1	0.0002	0.0002	8.51	0.05
AXD	1	0.0001	0.0001	3.79	
BXC	1	0.0001	0.0001	2.18	
BXD	1	0.0000	0.0000	0.24	
CXD	1	0.0001	0.0001	5.30	0.1
Error	5	0.0001	0.0000		
Total	15	0.0063			

TEST RUN 2 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0041	0.0041	22.84	0.01
B	1	0.0000	0.0000	0.15	
C	1	0.0114	0.0114	63.96	0.01
D	1	0.0000	0.0000	0.28	
AXB	1	0.0001	0.0001	0.53	
AXC	1	0.0000	0.0000	0.25	
AXD	1	0.0000	0.0000	0.07	
BXC	1	0.0001	0.0001	0.43	
BXD	1	0.0004	0.0004	2.12	
CXD	1	0.0000	0.0000	0.15	
Error	5	0.0009	0.0002		
Total	15	0.0171			

TEST RUN 3 - FLEXIBLE ASSIGNMENT

	df	SS	MSE	F	Significance
A	1	0.0023	0.0023	3.79	
B	1	0.0000	0.0000	0.02	
C	1	0.0011	0.0011	1.75	
D	1	0.0027	0.0027	4.49	0.1
AXB	1	0.0002	0.0002	0.29	
AXC	1	0.0002	0.0002	0.32	
AXD	1	0.0003	0.0003	0.49	
BXC	1	0.0003	0.0003	0.47	
BXD	1	0.0000	0.0000	0.03	
CXD	1	0.0023	0.0023	3.87	
Error	5	0.0030	0.0006		
Total	15	0.0125			

icantly affected. Interestingly, stepper disqualification rate becomes significant only under P2. This is due to the fact that under P1, since the number of test runs required are low, so are the number of reworked wafers and it does not make any significant contribution. For P3, the number of test runs required are high, but the lead time at PL is so low that the increase in number of reworked lots does not affect cycle-time performance.

The ANOVA table for the coefficient of variation of the cycle-time is given in Table VI. Adverse affect of breakdowns on the variability on cycle-time is again reduced or eliminated when flexible is adopted instead of the dedicated machine assignment policy. For P3, as the variability of cycle-time is very low, none of the factors significantly contribute to its variation, except for breakdowns under dedicated machine assignment. Variability of cycle-time under P1 is strongly affected by the inspection time, the breakdowns, the test run frequency.

Tables VII and VIII depict ANOVA results for the mean and the coefficient of variation of lead time during PL. The factors that have been found to be significant for the overall cycle-time are significant for lead time during PL as well. This result, however, strongly supports the opinion that any attempt to reduce the lead time at PL reduces the overall fab cycle-time.

VII. CONCLUSION

In our study, we consider several process control policies and process factors for the PL process in a DRAM manufacturing facility and examine their effects on cycle-time performance via a simulation study. We have shown that P3, where the test wafer is being inspected while the lot is being processed, performs best in terms of cycle-time. P2, where the lot is processed after the test wafer is inspected and the failed wafers are not matched with their original lots, but are used to form new lots after stripping, is the second best in terms of performance measure. However, in case of quality problems, the original lot with the defect might not be easy to trace. For P1, this is not an issue, since all wafers move together during the entire fabrication, but this policy has the worst cycle-time performance.

From these results, it appears that, to mitigate the adverse effects of test run policies, semiconductor manufacturers could be compelled to alternate between different test run policies. Rather than using a single test run policy at all times, a fab might be compelled to switch between P1 and P3, depending on the inventory level. If the WIP level is high, then P1 may be invoked to take advantage of its ability to process several lots after a reticle setup. When WIP levels are low, P3 may be used. However, it is disputable whether this is the best strategy. When the WIP level is high, faster processing rates are required to avoid extremely long cycle-times. By using P1, and increasing the lead time at PL, the cycle-time performance might be degraded. Therefore, parallel testing, P3, seems to be the best policy under all circumstances.

The inspection time has the most significant effect on cycle-time performance. Type of breakdowns (i.e., short but frequent as opposed to long but seldom) is the other most significant factor, but if a flexible machine assignment policy can be adopted, its adverse effects may be reduced. Stepper disqualification rate becomes significant only under P2. Test run frequency is significant for both P1 and P3.

These results have several implications for all the parties in the market. The fact that the duration of inspection time significantly affects the cycle-time performance puts pressure on inspection device manufacturers to strive for new equipment designs that reduce inspection time. Furthermore, if quality issues force device manufacturers to use P1, PL equipment manufacturers have to improve the optical accuracy of their equipment to produce high-quality products that conform to the tight tolerance specifications of the new device technologies. Finally, the semiconductor manufacturers have to refine the manufacturing process to reduce stepper disqualification rate.

This study constitutes a benchmark study modeling the complexities of PL and displays its significance on the overall system performance. It could be extended to examine whether there is any value to change between test run policies at different WIP levels in terms of cycle-time performance. Also, the flexible assignment policy clearly reduces cycle-time. However, there is no statistical model in literature that predicts the yield loss under flexible assignment. Such a model could provide manufacturers with valuable information. Another area of interest is how these results generalize to ASIC fabs with a diverse product mix. We conjecture that as long as the dedication issue remains, much of these results remains valid, but this needs to be explored systematically using realistic data.

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REFERENCES

[1] A. M. Law and W. D. Kelton, *Simulation Modeling and Analysis*, 2nd ed. New York: McGraw-Hill, 1991.
[2] R. C. Leachman, "The competitive manufacturing survey: Second report on results of the main phase," Univ. California, Berkeley, 1994.
[3] D. J. Miller, "Simulation of a semiconductor manufacturing line," in *Proc. 1989 Winter Simulation Conf.*, 1989, pp. 922–929.
[4] T. C. McGuigan, "Modeling the lot selection process in semiconductor photolithography processing," in *Proc. 1992 Winter Simulation Conf.*, 1992, pp. 885–889.
[5] C. D. Pegden, D. R. Shannon, and R. Sadowski, *Introduction to Simulation Using SIMAN*, 2nd ed. New York: McGraw-Hill, 1995.
[6] K. Prasad, "A generic computer simulation model to characterize photolithography manufacturing area in an IC FAB facility," *IEEE Trans. Components, Hybrids, Manufacturing Technol.*, vol. 14, pp. 483–487, 1991.
[7] J. M. Przybyla, J. Williams, and T. Joy, "A fully integrated photolithography workcell," in *IEEE/SEMI Int. Semiconductor Manufacturing Science Symp. '89 Proc.*, 1989, pp. 100–107.
[8] A. M. Spence and D. J. Welter, "Capacity planning of a photolithography work cell in a wafer manufacturing line," in *Proc. IEEE Conf. Robotics and Automation*, 1987, pp. 702–708.
[9] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era—Volume 1: Process Technology*. Sunset Beach, CA: Lattice Press, 1986.
[10] A. M. Zargar, "Effect of rework strategies on cycle time," *Computers in Industrial Eng.*, vol. 29, pp. 239–243, 1995.

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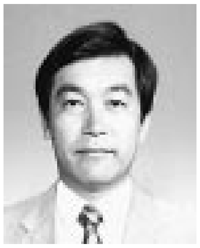

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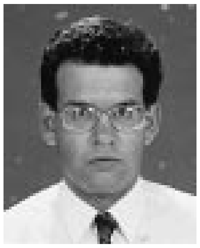

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